Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.115”**

**.115”**

**ANODE**

**.085”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .085” X .085”**

**Backside Potential: CATHODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .115” X .115” DATE: 11/10/21**

**MFG: SUSSEX THICKNESS .013” P/N: 1N6303**

**DG 10.1.2**

#### Rev B, 7/1